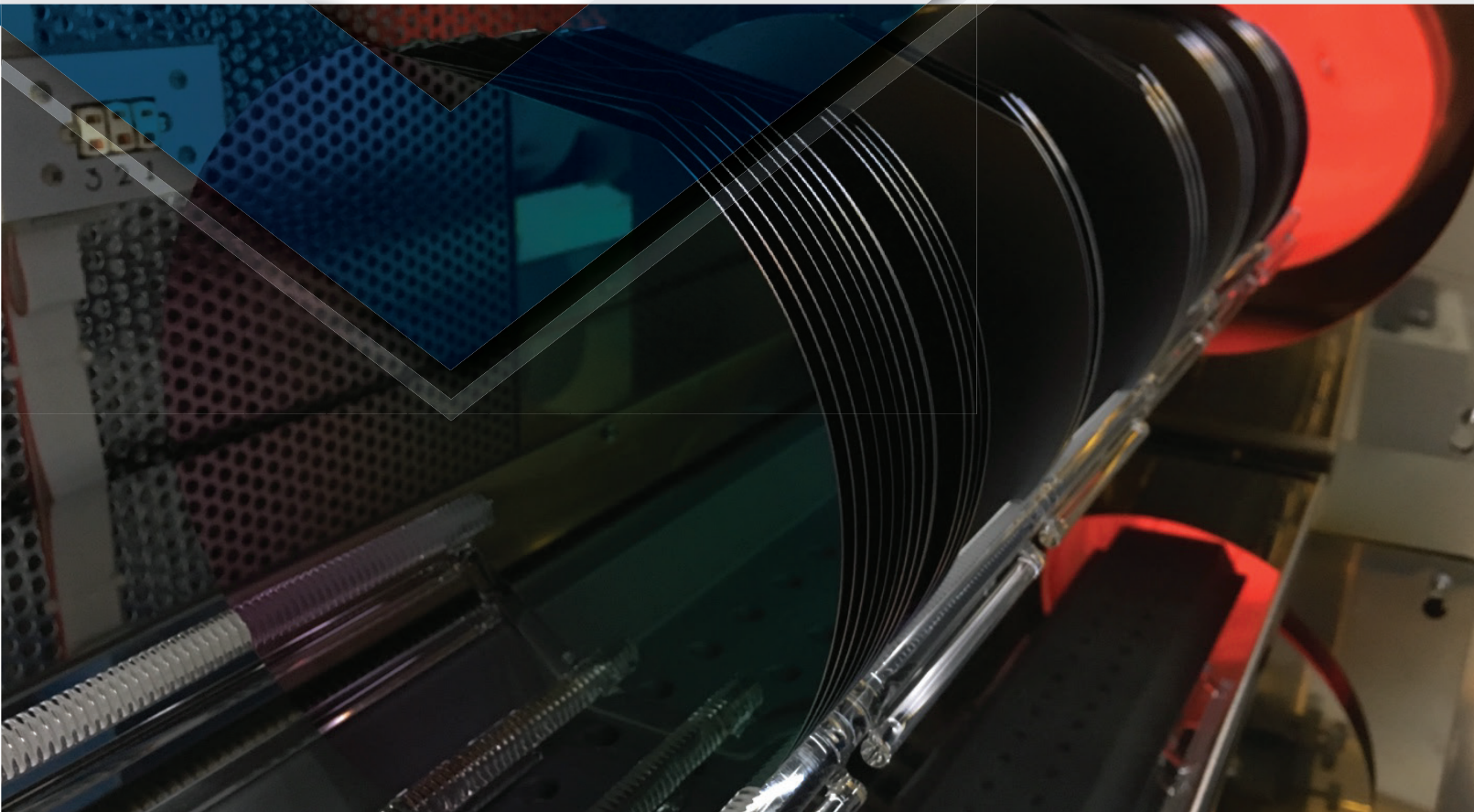
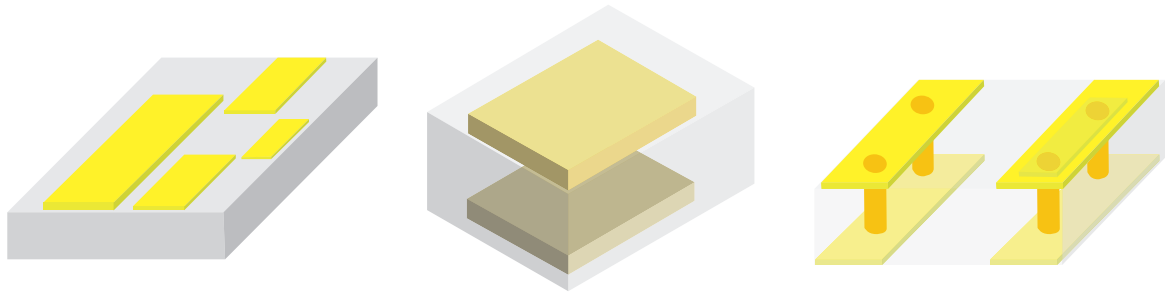




Power & Lighting Semiconductor Co., Ltd. (P&L Semi) is a pioneer and a top class Semiconductor Manufacturer of silicon chips and devices. With 25 years of semiconductor manufacturing experience, strict standards of quality, constant improvements in R&D, technology, and processes, and the hard work of a team of dedicated professionals, P&L Semi today is a Korea brand that is recognized globally.



Custom Substrate Submount for Heat sink



CAPABILITES

- Conductor patterning on 2 surfaces
- Wire bonding or paste attach or eutectic metallization
- Conduction by via hole
- Tight dimensional tolerance

APPLICATIONS

- All electro device applications for heat sink
 - Laser, Optical, VCSEL(TOSA/ROSA)
- Applications that require simplification circuit

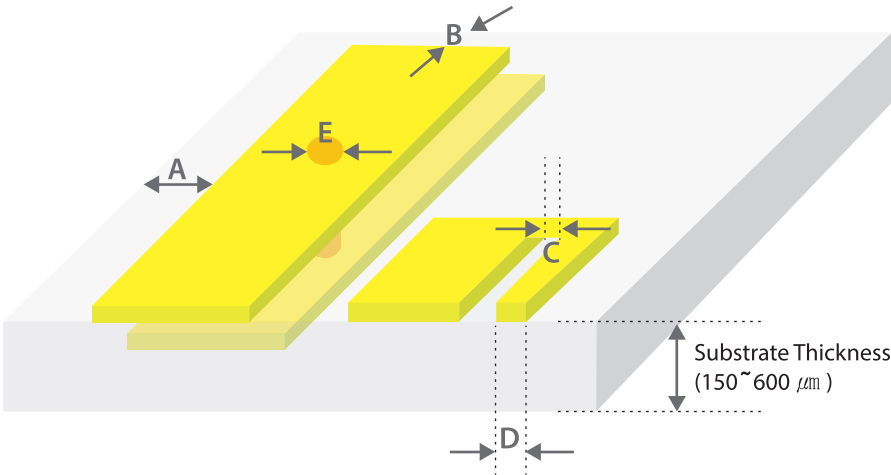
DESIGN RULES AND SPECIFICATIONS

- Substrate materials : Silicon / Al₂O₃ / AlN / SiC / BeO / Copper available
- Metallization : Ti / Pt / Au / Sn / Pd / Ag / Cu / AuSn metallization available
- Substrate thickness : Between 150 μm to 600 μm
- Minimum pattern cap : 20 μm
- Metal pattern to diced edge Tolerance : ≥ 20 μm

DESIGN SPECIFICATION

Substrate	Silicon / Al2O3 / AlN / SiC / BeO / Copper			
Via Hole type substrate	Al2O3 / AlN			
Via Hole size	See list below			
unit : μm				
Substrate Thickness	150~250	300~400	400~500	500~600
Standard Via Diameter (Top / Bottom)	80 / 60 ± 15	100 / 80 ± 15	120 / 100 ± 15	180 / 150 ± 15
Saw line width	100 ± 15	110 ± 15	140 ± 15	200 ± 15
Substrate thickness	150 μm to 600 μm			
Minimum pattern cap	20 μm			
Metal pattern to diced edge Tolerance	≥ 20 μm			
Metal system	All Metal E-Beam Deposition (except via hole)			
Metallization	Ti / Pt / Au / Sn / Pd / Ag / Cu / AuSn			
Standard AuSn solder composition	Au:Sn=70:30 wt% $\pm 2.5\%$			

PATTERNING DESIGN RULES



A	B	C	D	E
SAW LINE WIDTH	REMAINING SAW	PATTERN TO PATTERN DISTANCE	METAL WIDTH	VIA HOLE SIZE
Silicon : min 25 μm Al ₂ O ₃ /AlN/SiC/ Copper:min 50~100 μm	AFTER DICED MAXIMUM 10 μm	MINIMUM 10 μm	MINIMUM 10 μm	PLEASE SEE THE DESIGN SPECIFICATION

DESIGN RULES AND SPECIFICATIONS

<u>P</u>	<u>S</u>	<u>S</u>	-	<u>2</u>	<u>0</u>	<u>7</u>	<u>4</u>	<u>0</u>	<u>3</u>	<u>9</u>
①	②	③		④	⑤					

- ① P&L
- ② SEMICONDUCTOR
- ③ Substrate materials - S : Silicon / O : Al2O3 / A : AlN / C : SiC / B : BeO / P : COPPER
- ④ IF symbol is 1 = Insulation Type, IF symbol is 2 = Conduction Type
- ⑤ DESIGN CHIP SIZE (UNIT : μm)
ex) IF DESIGN NUBMER IS 074039 = 740X390 μm

Custom Substrate

Submount for Heat sink

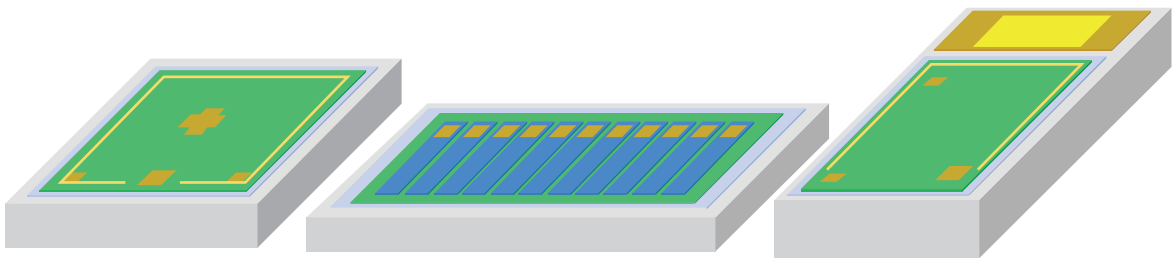
MATERIAL PROPERTIES

PROPERTIES	AlN	Al ₂ O ₃	Si (Conductivity Type)	Si (Insulated Type)	BeO	SiC
Bulk Density (kg / m ³)	3.3	3.8	2.4	2.4	3.02	3.21
Thermal expansion coefficient (×10 ⁻⁶ K)	4.5	7.2	3.5 (RT~100°C)	3.5 (RT~100°C)	9	4~5
Thermal conductivity (W/m K , RT)	≥200	35	145	145	285	390
Volume resistivity (Ωcm, RT)	>10 ¹³	>10 ¹³	0.01	1,000	>10 ¹⁵	>10 ⁵
Dielectric constant (1MHz, RT)	9.2	10	11.9	11.9	6.8	~9.66
Bending Strength (Mpa, RT)	343	294			150	

MATERIAL PROPERTIES

Material	Resistivity Coefficient	Temperature	Conductivity
	- ρ -	Coefficient	- σ -
	(ohm-m)	per degree C	(1 /Ωm)
Aluminum	2.65 x 10-8	3.8 x 10-3	3.77 x 107
Copper	1.724 x 10-8	4.29 x 10-3	5.95 x 107
Gold	2.24 x 10-8		
Platinum	10.5 x 10-8	3.93 x 10-3	0.943 x 107
Tin	11.0 x 10-8		
Au(80%)Sn(20%)	8.61x 10 ⁻⁷		

Si PHOTO DIODE



CAPABILITES

- Sensitive in the UV to near IR range
- Sensitive in the Visible to near IR range.
- RGB color sensor
- Low dark current
- Laser beam detector

APPLICATIONS

- Barcode readers & Remote control
- Laser, Optical, VCSEL(TOSA/ROSA)
- Applications that require simplification circuit
- Vehicle Information and control & LED display

DESIGN RULES AND SPECIFICATIONS

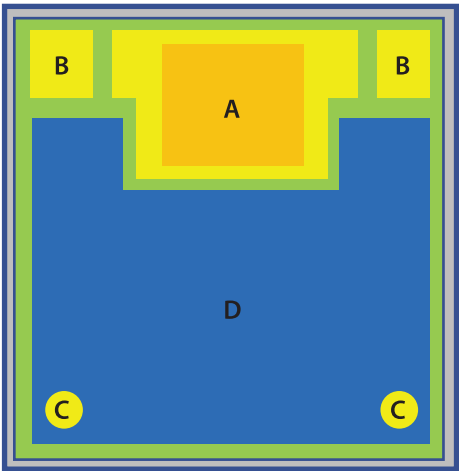
- Substrate materials : Silicon available
- Metallization : Ti / Cr / Au / Sn / Ag / AuSn metallization available
- Substrate thickness : Between 100 μm to 650 μm

DESIGN SPECIFICATION

Substrate	Silicon
Substrate thickness	100 μm to 650 μm
Metallization-TOP	Al / Au / Ag / AuSn
Metallization-Bottom	Au / Ag / AuSn
Metal system	All Metal E-Beam Deposition
Standard AuSn solder composition	Au:Sn=70:30 wt% $\pm 2.5\%$
Passivation	Silicon Oxide or Silicon Nitride

Si PHOTO DIODE

SUBMOUNT ON SILICON PHOTO DIODE



A	B	C	D
Eutectic area	Wire bonding area	Wire bonding area	Photo diode surface
Used AuSn Metal	LD Bonding pad	PD Bonding pad	Received Light Area

DESIGN RULES AND SPECIFICATIONS

<u>P</u>	<u>S</u>	<u>D</u>	-	<u>1</u>	<u>0</u>	<u>8</u>	<u>5</u>	<u>0</u>	<u>9</u>	<u>0</u>
①	②	③		④	⑤					

- ① P&L
- ② SEMICONDUCTOR
- ③ PHOTO DIODE
- ④ IF symbol is 1 = P up, IF symbol is 2 = N up
- ⑤ DESIGN CHIP SIZE (UNIT : μm)
ex) IF DESIGN NUBMER IS 085090 = 850X900 μm

CONTACT INFORMATION

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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Maximum rating	Unit
Reverse Breakdown Voltage	BV _R	30	V
Junction Temperature	T _J	150	°C

ELECTRICAL / OPTICAL CHARACTERISTICS (Ta = 25°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open Circuit Voltage	V _{OP}	Note(1)	0.3	0.4	-	V
Short Circuit Current	I _{SC}	Note(1)	CUSTOMIZED			μA
Spectrum Sensitivity	λ		300 ~ 1,100 CUSTOMIZED			nm
Peak Sensing Wavelength	λ _P		CUSTOMIZED			nm
Forward Voltage	V _F	I _F =10 mA	0.5		1.3	V
Dark Current	I _D	V _R =10V		5	10	nA
Reverse Breakdown Voltage	BV _R	I _R =10 μA	30	-	-	V

Note(1):Parallel light of 1,000Lux illumination is applied by a Tungsten lamp of 2856k.



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